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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,439	12/28/2001	Eleanor P. Rabadam	42P12399	8983

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EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

8M

Office Action Summary	Application No.	Applicant(s)	
	10/039,439	RABADAM ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-17,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13-17,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/18/05 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 6, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Humphrey et al. 6,476,486 B1 in view of Mart et al. 5,563,838 in view of Lee et al. 5,917,757. Humphrey discloses (see, for example, Fig. 8) an integrated circuit mounting package comprising a ball grid array (power supply in package (PSIP) device) 10, an integrated circuit die 20 and electronic device (passive component) 37. In column 2, lines 34-43, Humphrey discloses the electronic device may be a voltage regulator. Humphrey does not specifically state the integrated circuit die including a memory array. However, it was extremely well known in the art at the time of invention that integrated circuit dies include memory arrays. Mart teaches (see, for example, column 1, lines 28-39) that integrated circuit chips come in a variety of forms, i.e.

DRAM, SRAM, ROM, gate arrays, etc., which are all types of memory chips. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have a memory array in order to form a memory chip device, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Humphrey in view of Mart does not disclose the voltage regulator circuit to provide a programming voltage potential to the memory array. However, Lee discloses (see, for example, column 4, lines 27-42) a voltage pump circuit being coupled to a voltage regulator for supplying a variety of voltages to a memory. It would have been obvious to one of ordinary skill in the art at the time of invention to have the voltage regulator circuit to provide a programming voltage potential to the memory array in order to create the needed voltage for necessary functions of a memory.

4. Claims 2 thru 4, 7 thru 10, and 14 thru 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Humphrey et al. '486 B1 in view of Mart et al. '838 in view of Lee et al. '757 as applied to claims 1, 6, and 13, and further in view of Spielberger 6,005,778. Humphrey in view of Mart in view of Lee does not disclose the passive component being mounted to the integrated circuit die with an epoxy material. However, Spielberger states (see, for example, column 4, lines 40-42 and column 4, lines 12-17) that a chip is bonded by a conductive or nonconductive adhesive, and that epoxies are an example of adhesives. It would have been obvious to one of ordinary skill in the art at the time of invention to use an epoxy material in order to stabilize the passive component on the integrated circuit die.

Regarding claim 3, Humphrey in view of Mart in view of Lee in view of Spielberger discloses the claimed invention except for the epoxy material between the passive component and the integrated circuit die being less than about 0.050 millimeters in thickness. However, it was well known in the art at the time of invention to use this thickness in order to reliably attach one semiconductor component to another component in a semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to use an epoxy material being less than about 0.050 millimeters in thickness, in order to reliably attach the chip to the voltage regulator, and since it has been held that discovering an optimum value of a result effective value involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claims 8-10, Humphrey in view of Mart in view of Lee does not disclose wires to connect the integrated circuit or passive component to the substrate. However, Spielberger discloses (see, for example, left side of Figure 5) wires (first wire bond) 28a that connect the integrated circuit 40b to substrate 14b. For claims 9 and 10, Spielberger discloses (see, for example, right side of Figure 5) other wires (second wire bond) 28a that connect the passive component to the substrate. It would have been obvious to one of ordinary skill in the art at the time of invention to include these wires in order to make a reliable connection between the integrated circuit or passive component to the substrate.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Humphrey et al. '486 B1 in view of Mart et al. '838 in view of Lee et al. '757 as applied to claims 1, 6, and 13 above, and further in view of Klughart 6,396,137 B1. Humphrey in view of Mart in view of Lee

does not disclose the passive component including at least one of a capacitor and an inductor. However, Klughart discloses (see, for example, FIG. 26) a device comprising a capacitor 2611 on top of a voltage regulator 2607. In column 34, lines 17-42, Klughart discloses that parasitics are eliminated. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the passive component including at least one of a capacitor and an inductor in order to eliminate parasitics.

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Humphrey et al. '486 B1 in view of Mart et al. '838 in view of Lee et al. '757 as applied to claims 1, 6, and 13, and further in view of Javanifard et al. 6,385,033 B1. Humphrey in view of Mart in view of Lee does not disclose the integrated circuit die including a flash memory array. However, it was very well known in the art that flash memory arrays were one of many types of memory arrays utilized in memory chips. Javanifard discloses (see, for example, column 6, lines 9-15) a memory circuit device comprising a flash memory. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a flash memory in order to utilize a common memory array that capably reads, writes, and stores data in a semiconductor device.

7. Claims 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Humphrey et al. '486 B1 in view of Mart et al. '838 in view of Lee et al. '757 as applied to claims 1, 6, and 13, and further in view of Takai et al. 6,352,880 B1. Humphrey in view of Mart in view of Lee does not disclose an encapsulant at least partly encapsulating the integrated circuit die and the passive component. However, Takai discloses (see, for example, FIG. 1) a device

comprising a chip 11, and resin sealing material (encapsulant) 14. The encapsulant protects the chip from the environment. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have an encapsulant at least partly encapsulating the integrated circuit die and the passive component in order to protect the integrated circuit.

Response to Arguments

8. Applicant's arguments with respect to claims 1-11, 13-17, 21, and 22 have been considered but are moot in view of the new ground(s) of rejection.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
May 30, 2005